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The Trend of Different Parameters for Designing Integrated Circuits from 1973 to 2019 and Linked to Moore's Law

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ABSTRACT

The number of transistors per chip, feature sizes, frequencies, transistor densities, number of cores, thermal design powers, die areas, and storage capacities of Integrated Circuits (ICs) used for different processing units and memories were collected from various websites from 1973 to 2019 and plotted against year of introduction of ICs in semi-log paper to find the trend with R-squared (R^2) value using Microsoft Excel. The R^2 values of the trend lines for the above parameters were over 0.922 which indicated that more than 92% of data satisfied the fitting lines except for thermal design power ($R^2 = 0.7$) and die area ($R^2 = 0.4$ to 0.6). It was observed that the growths of transistor counts, transistor densities, frequencies, and thermal design powers for different processing units were growing exponentially and doubled every 16.8 to 24 months from 1973 to 2019 except the growth of thermal design powers (TDP) and frequencies of ICs which were increased up to 2003. After that, the growth of TDP and frequencies are nearly linear up to the present day. The growth of the above parameters for ICs of different memories were a little faster, it was doubled every 14 to 16 months. The feature sizes shrunk 2 times every 18 months. A strong relation was found between feature sizes and transistor densities ($R^2 = 0.9$) and observed that one fold of feature size decreased for the increasing of 2-3 folds of transistor densities. It was observed that different parameters for ICs designing from 1973 to 2019 kept pace with Moore's law. It may be concluded that the decrease of feature size, increasing of transistor count and transistor density in ICs design will follow Moore's law for some more years with the limitation of frequency and power of ICs.

Keywords: Integrated circuits, Microprocessors, Transistors, Frequencies, TDP, Memories, and Moore's law.

INTRODUCTION:

Walter Brattain, John Bardeen, and William Shockley created the world's first transistor in 1947-1949 and begun the end of the vacuum tube used in electrical appliances (Wikipedia, 2020a). The first integrated circuit (IC) in the form of a flip flop was developed using 2 transistors by Jack Kilby in 1958 (Wikipedia, 2020b) and the Monolithic Silicon IC Chip was invented by Robert Noyce in 1961 (VLSI Res. Inc., 2020).

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The very-large-scale integration (VLSI) was started with hundreds of thousands of transistors in the early 1980s. Modern VLSI devices contain so many transistors, layers, interconnections, and other features and the application areas got expanded from micro-controller to Field-Programmable Gate Array (FPGA) based technologies, wireless mobile communications, and artificial intelligence (Padhy *et al.*, 2015; Islam and Hossain, 2019; Zamin *et al.*, 2012; Boddupalli, 2017; and Charles *et al.*, 1986).

Presently a modern IC consists of millions of transistors. During these 5 decades, the size, speed, and capacity of ICs have progressed enormously due to rapid advances in computer architecture and semiconductor technologies (Yung *et al.*, 2002). Almost anything related to the semiconductor industry would be approximated a straight line when plotted on semi-log paper, and the number of transistors on a chip, integration complexity, power of computers and processor speeds would be doubled about every 1 to 2 years (Moore, 1965; Vangie, 2020; and Bajramovic, 2013).

Moore's law is a projection of a historical trend so the growth rate might not be continued for an indefinite period. International Technology Roadmap for Semiconductor (ITRS) predicted that the growth would be slow around 2103 (Hoefflinger, 2011). Jorgenson *et al.* (2014) stated that Moore's law is dying in the next decade. Therefore, research was undertaken to examine the trend of different parameters for designing integrated circuits from 1973 to 2019 and linked to Moore's law.

MATERIALS AND METHODS:

Transistor counts, feature sizes, die areas, clock speeds, thermal design powers (TDP), number of cores, etc. of different type of processing units released from 1973 to 2019 by different manufactures (AKM, AMD, Fairchild, Fujitsu, General Instrument, General Microelectronics, Hitachi, Honeywell, Hyundai, IBM, Intel, Matsushita, Mitsubishi, NEC, NTT, Samsung, Sandisk, SDS, Seeq, Siemens, Signetics, Toshiba, Transatron) were collected from different websites (Wikipedia, 2020c; Wikipedia, 2020d; Martin, 2019; and Wikipedia, 2020e) and plotted these as a dependent variable against the year of introduction of ICs as an independent variable.

The capacities of Random-Access Memory (RAM), Read-Only Memory (ROM), and Flash Memories (FL) released by different manufacturers at various times were also collected from the above sources. Exponential trend lines with R-squared values of different parameters of ICs were plotted on semi-log paper with the Microsoft Excel program. R-Squared values were determined to observe the variation of a dependent variable with the independent variable. If the value of R^2 is very close to 1, the movements of the data of dependent variables are completely

explained by the movements of the year of introduction of ICs. The number of months was counted for 10 times increase or decrease from trend lines of different parameters of ICs to find the growth rates and linked to Moore's law.

RESULTS AND DISCUSSIONS:

There were 2300 transistors per chip for Intel-4004 in 1971 but it became 23.6 billion transistors per chip at Graphcore GC2 IPU in 2018 (Wikipedia, 2020c). Thus the number of transistors per chip for the Central Processing Unit (CPU) has been increased 9,440,000 times in 47 years. NEC developed μ PD7220-GDC graphics processing unit with 40,000 transistors in 1982 (Wikipedia, 2020c; Dampf, 1986) but Nvidia designed GV100 Volta Graphical Processing Unit (GPU) with 21.1 billion transistors per chip in 2017 (Wikipedia, 2020c).

Xilinx Virtex developed a Field-Programmable Gate Array (FPGA) with 70,000,000 transistors per chip in 1997. At the end of 21 years, Xilinx Everest designed an FPGA with 50 billion transistors per chip (Cutress, 2018). Two thousand three hundred transistors per chip were at Intel4004 in 1971 but it reached 50 billion at FPGA Xilinx Everest in 2018. Thus the transistor count has increased 21,739,130 times in 47 years. The number of transistors and their trends over time for early ICs, CPU, GPU, and FPGA is shown in **Fig 1**.

It is also observed from the **Fig 1** that the transistor counts for all types of processing units are increased exponentially. The R^2 values of exponential lines of CPU, GPU, and FPGA are 0.930, 0.961, and 0.958 respectively. These results indicate that more than 93% of data follow the movement of exponential trend lines. It was also found that the number of transistors doubled every 18.00, 17.76, and 20.40 months for CPU, GPU, and FPGA respectively. These results indicate that the transistors' growth per chip is still following Moore's law.

The number of transistors per chip, feature sizes, and die areas for CPU, GPU, and FPGA were plotted on semi-log paper against the year of introduction of ICs and found the exponential trend lines (**Fig 2**). It is observed that the exponential trend lines fit strongly for transistor count ($R^2 = 0.953$) and feature size ($R^2 = 0.980$). However, the die area does not fit

well ($R^2 = 0.387$) with the exponential trend line. The process technology or feature size has rapidly shrunk from 10,000 nm at Intel4004 in 1971 to 5 nm at Samsung 5LPE in 2019 (Scotten, 2018). Transistors were doubled every 16.8 months and

feature size was decreased by 2 folds each 18 months. Thus the feature size has been decreased 2000 times in 48 years. The above results also hold Moore's law for various parameters of ICs except die area.

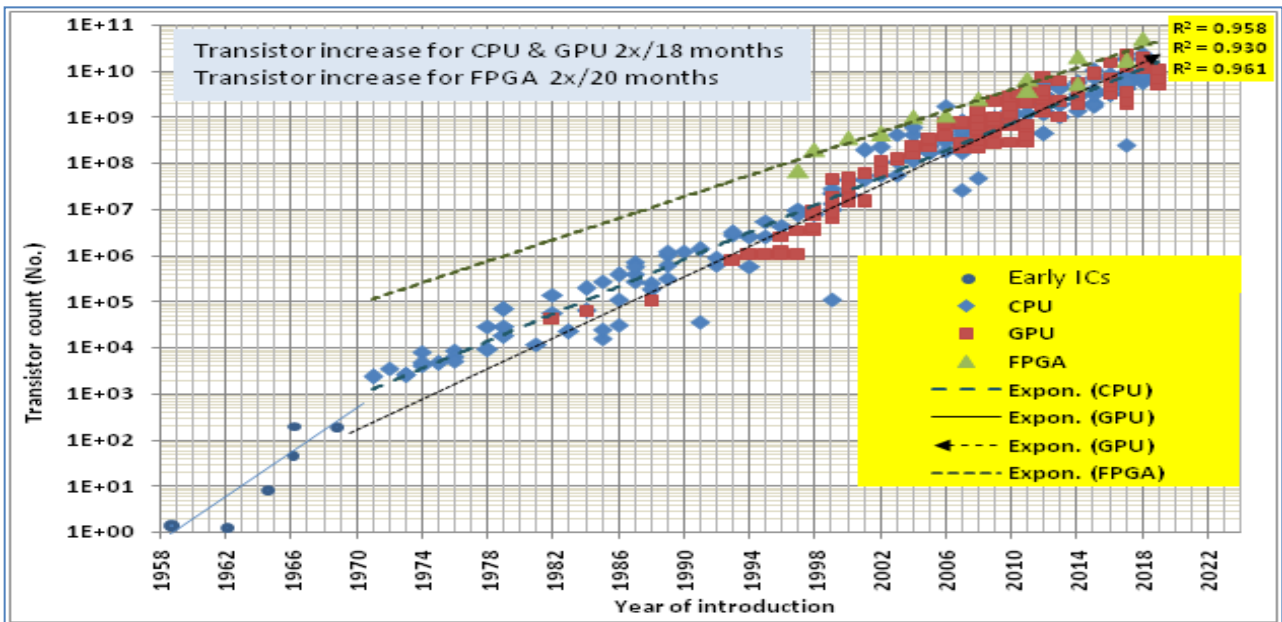


Fig 1: The number of the transistor count of CPU, GPU, and FPGA as a function of time.

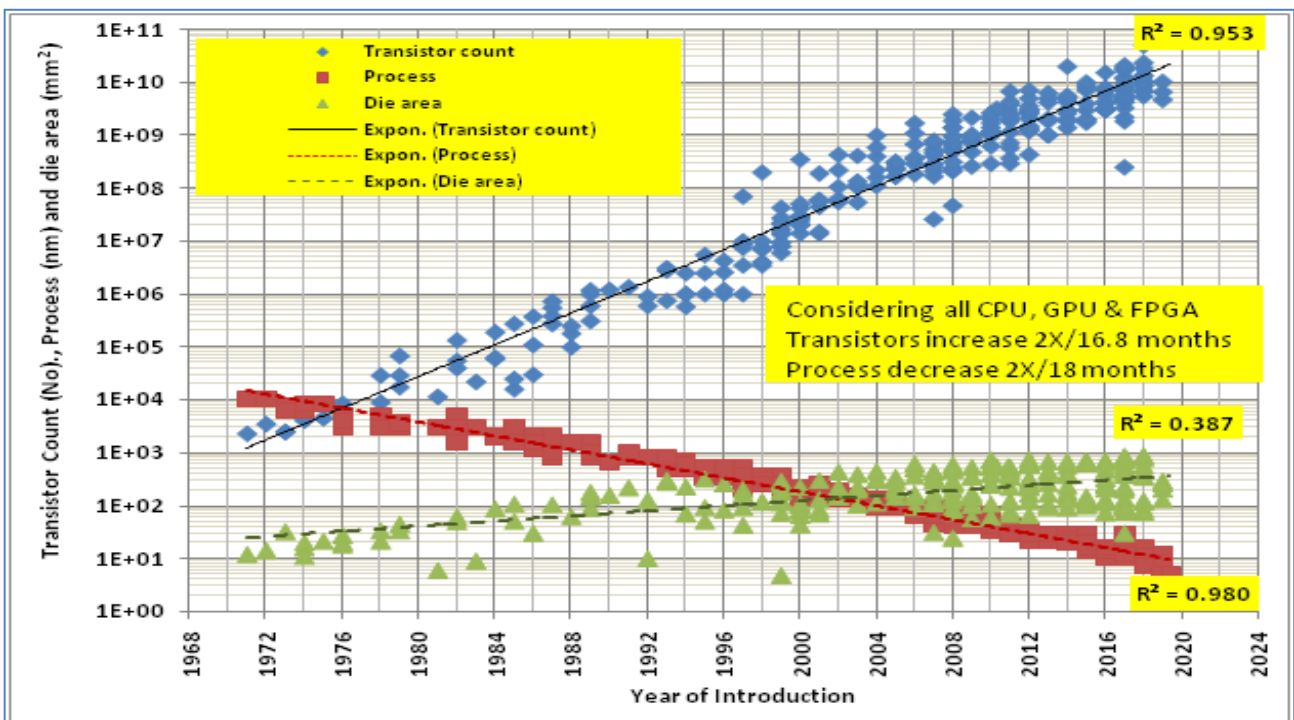


Fig 2: Transistors count, feature size, and die area of various processing units over time.

The exponential trend line of transistor densities (TD) for CPU, GPU, and FPGA against release date of ICs was determined (Fig 3) and it was found that TD was doubled every 28 months for considering data from 1969 to 2019. However, the transistor

densities were doubled every 18 months when data were considered from 1987 to 2019. This result indicates that Moore's law is still applicable to the growth of transistor densities. An excellent relation ($R^2 = 0.984$) was found between the feature size and

transistor densities for CPU, GPU, and FPGA. It was found that 1 fold of feature size was decreased for the increasing of 2 times of transistor densities (Fig 4).

The frequencies, TDP, and the number of cores per die were plotted as a function of the introduction year for different integrated circuits. There was only 1 core per die in ICs for a long time (from 1972 to 2004). It was reached to 10 cores per die in the next 6 years and 56 cores per die by Intel for developing

Xeon Platinum in 2019. The TDP of ICs was increased exponentially up to 2005 and doubled two times each 24 months. After that, the growth of TDP is linear up to today. The frequency of the ICs was 108 kHz in 1972 but it was increased exponentially ($R^2 = 0.965$) up to the year 2005 and doubled every 20.4 months. However, the growth of frequency is linear as same as the power of ICs from 2006 to the present date. The frequency was increased 25925 times from 1972 to 2004 but it was increased only 0.96 times in the next 15 years, Fig 5.

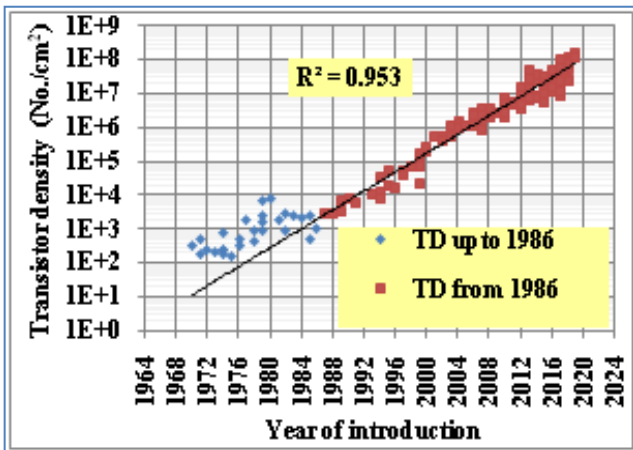


Fig 3: Transistor density (TD) of CPU, GPU, and FPGA versus year of the first release of ICs.

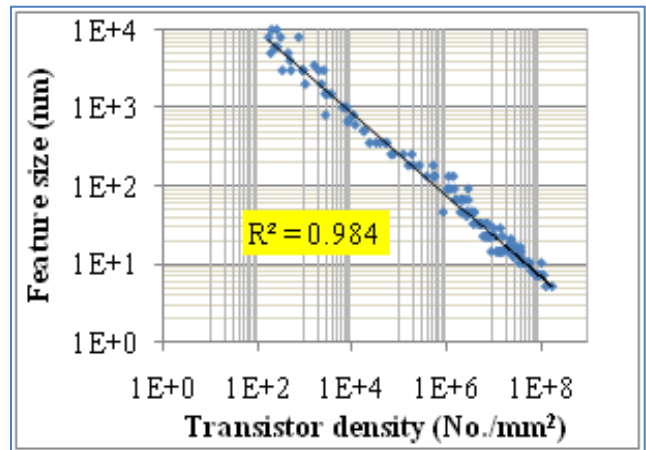


Fig 4: Transistor density versus feature size of CPU, GPU, and FPGA.

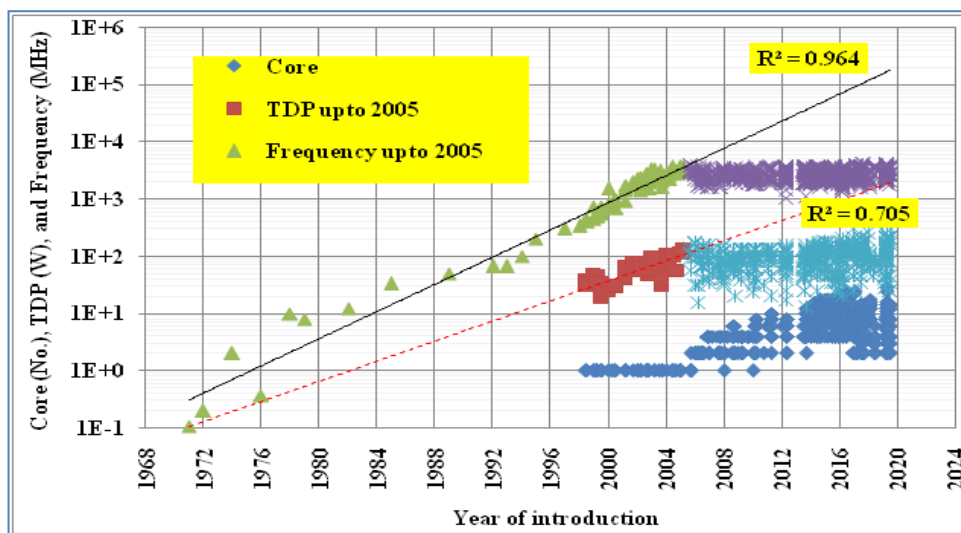


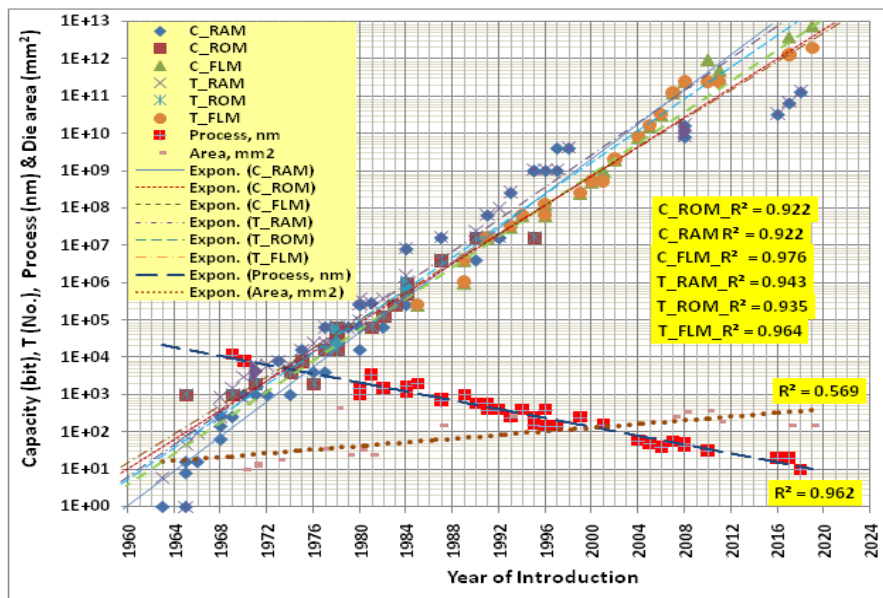
Fig 5: Frequencies, TDPs, and cores per die of different ICs versus year of the first release.

Transistor counts, feature sizes, die areas, and capacities of different types of memories (RAM, ROM, and Flash) released by various manufacturers were collected from the Wikipedia, 2020c). Fairchild developed an SRAM type RAM with 6 transistors and 1 bit capacity in 1963 (Wikipedia, 2020c; 1966: Semiconductor, 2019). The capacity of RAM was reached at 128 Gb with 137 billion transistors at 10

nm feature size by Samsung in 2018 (Wikipedia, 2020c; Liu, 2018). The capacity of RAM has increased 128 billion times in 55 years. MOS type 1 Kilobyte (Kb) capacity ROM Memory with 1024 transistors was introduced by General Microelectronics in 1965 (Wikipedia, 2020c). AKM and Hitachi released ROM of 16 megabyte (Mb) capacity by adding 16.7 million transistors in 1995

(Wikipedia, 2020c). The flash memory of 256 Kb capacities was marketed by Toshiba in 1985. The number of the transistor of the flash memory was 262144 and 2000 nm processing technology was used in the IC. After 4 years, in 1989, Intel released a flash memory with 1 Mb capacity. In 2019, the capacity of the flash memory is reached to 8 Terabyte (TB) capacities where 2048 billion transistors are added by Samsung. The R^2 value of exponential trend lines for all parameters of memories is larger than 0.922 except the trend line of die area ($R^2 = 0.569$). **Fig 6** shows the trends in memory complexity. The capacities of RAM, ROM, and Flash memories were double every 15.88, 15.64, and 13.48 months respectively.

The transistor densities of memories were plotted against the year of introduction (**Fig 7**) and find the exponential trend line ($R^2 = 0.968$). **Fig 7** shows the relation between transistor densities of memories and the year of introduction. It was found that the transistor density doubles every 15.12 months and holds Moore's law. A strong relation was found between transistor count and processing technology of the ICs of different memories ($R^2 = 0.957$). The feature size was decreased sharply with the increase of transistor count (**Fig 8**). It was found from the trend line that the feature size reduced 1 fold per 3 time's increase of transistor count. The characteristic of trend lines of different parameters of ICs and linked to Moore's law is presented in **Table 1**.



(C = Capacity of memory in bits, T = Transistor count of different memories, & FLM =Flash memory)

Fig 6: Capacity, transistor count, feature size, and die area of various memories over time.

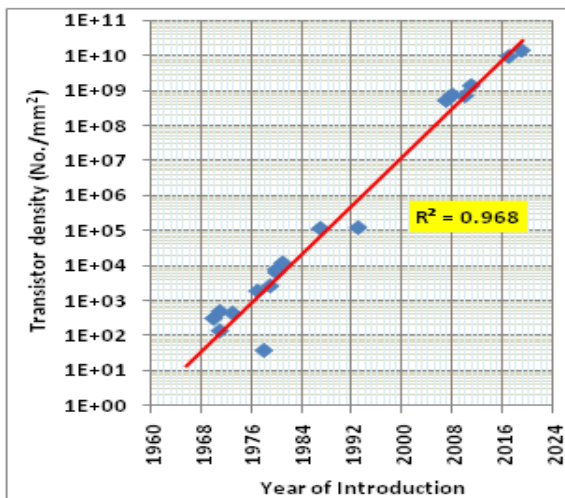


Fig 7: Transistor density for various memories versus year of the first release.

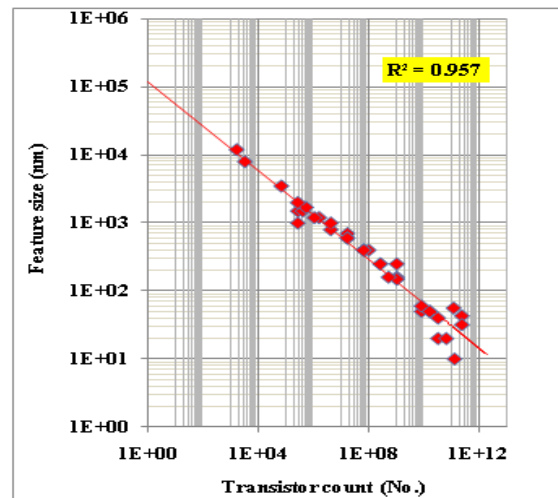


Fig 8: Feature size versus the transistor count of various memories.

Table 1: The characteristic of trend lines of different parameters of ICs and linked to Moore’s law.

Parameters of ICs	R ²	Time	Linked to Moore’s law
Transistor count for ICs of CPU vs. year	0.930	18.00 *	Hold to this date
Transistor count for ICs of GPU vs. year	0.861	17.76*	Hold to this date
Transistor count for ICs of FPGA vs. year	0.958	20.40*	Hold to this date
Transistor count for ICs of CPU, GPU and FPGA vs. year	0.901	16.80 *	Hold to this date
Transistor count for ICs of RAM vs. year	0.943	14.00 *	Hold to this date
Transistor count for ICs of ROM vs. year	0.935	14.20*	Hold to this date
Transistor count for ICs of Flash Memory vs. year	0.964	14.20*	Hold to this date
Transistor densities for ICs of for CPU, GPU and FPGA vs. year	0.953	18.00*	Hold to this date
Transistor densities for ICs of memories vs. year	0.968	18.00*	Hold to this date
Capacity of RAM vs. year	0.922	15.88*	Hold to this date
Capacity of ROM vs. year	0.922	15.64*	Hold to this date
Capacity of Flash memory vs. year	0.976	13.48*	Hold to this date
Frequency vs. year	0.963	18.72*	Hold up to 2005 then nearly no growth up to 2019
Power vs. year	0.788	24.00*	
Feature size for ICs of CPU, GPU and FPGA vs. year	0.980	18.00^	Hold to this date
Feature size for ICs of memories vs. year	0.962	38.40^	Does not follow
Die area for ICs of CPU, GPU and FPGA vs. year	0.387	96.00*	Does not follow
Die area for ICs of memories vs. year	0.569		Does not follow
Feature size vs. Transistor density for ICs of CPU, GPU and FPGA	0.984	Feature size decreased 1 fold/2 times increase of transistor densities	
Feature Size vs. Transistor density for all types of memories (RAM, ROM and Flash Memory)	0.957	Feature size decrease 1 fold/3 times increase of transistor densities	

*Months to increase for 2 folds ^ Months to decrease for 2 folds

CONCLUSION:

The R² values of the trend lines of transistor counts for various microprocessors and memories were varied from 0.86 to 0.96 which indicated that more than 86% of data satisfied the fitting lines to follow the movement with year of IC introduction. From the trend lines, it was also found that the number of transistors for various ICs was growing exponentially from 1973 to 2019 and doubling every 14 to 21 months which indicated keep pace with Moore's law. The exponential trend line of transistor densities of ICs for CPU, GPU, and FPGA (R² = 0.96) showed that it doubles every 28 months for considering data from 1973 to 2019 but it doubled in every 18 months when data were considered from 1987 to 2019. This result indicates that Moore's law is still applicable for transistor densities. The fitting line of transistor densities of various ICs for memory (R² = 0.968) showed that it was doubling every 15 months. The trend line of feature-size of different processing units (R² = 0.98) showed that it shrunk 2

times every 18 months and indicated keep pace with Moore's law while those for the ICs of memories (R² = 0.962) shrunk 2 times every 38 months. An excellent relation was found between the feature size and transistor densities. The trend lines (R² > 0.957) showed that the feature size decreased by 1 fold per 2-3 times of transistor densities for different ICs. The power and frequency were double every 19 to 24 months up to 2003 after that the growths were nearly linear to the present date. Even high-end processors have stopped increasing their clock speeds (Fox, 2018) due to the "Power Wall-a barrier to clock speed" (Blank, 2018). The process of technology rapidly decreased from 10,000 nm in 1971 to 5 nm in 2019. It shrinks 2 times every 18 months and indicates keep pace with Moore's law up to this date. Samsung and TSMC have planned to manufacture 3 nm GAAFET nodes by 2021–2022 (Armasu, 2019). Moore's law might exist in the next few years since the transistor count is increasing and the feature size is decreasing. However, high power

dissipation becomes a critical barrier to the frequency and performance of the microprocessor. It may be concluded that the decreasing of feature size and increasing transistor counts, transistor densities would continue some more years as also predicted by different researchers (Eide, 2018).

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CONFLICTS OF INTEREST:

The authors declare they have no competing conflict of interests with respect to the publication of the present research.

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